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EXAMINER	
MIYOSHI, JESSE Y	

ART UNIT	PAPER NUMBER
2811	

NOTIFICATION DATE	DELIVERY MODE
10/27/2010	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

mailroom@bskb.com

Office Action Summary	Application No.	Applicant(s)	
	10/564,486	SON, HYO-KUN	
	Examiner	Art Unit	
	JESSE Y. MIYOSHI	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 August 2010*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *33,34,37-42,44 and 47-57* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *33,34,37-42,44 and 47-57* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 42, 44, 47-50, 55-57 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

There is no support in the specification, as filed, for the claimed limitation of "the active layer is grown at a fourth temperature of 600~800°C higher than the first temperature" as recited in claim 42.

Claim Objections

3. Claim 42 is objected to because of the following informalities: the last line of claim 42 should recite "lower than the second temperature and the third temperature". Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 33, 34, 37-41 and 51-54 are rejected under 35 U.S.C. 103(a) as being unpatentable over Emerson et al. (US PGPub 2003/0006418; hereinafter "Emerson") in view of Vaudo et al. (U.S. 6,440,823; hereinafter "Vaudo").

Re claim 33: Emerson teaches (e.g. figure 1) a light emitting diode (LED), comprising: a first gallium nitride layer (**14**) having a first conductivity (n-type); a super lattice structure (**16**) including InGaN on the first gallium nitride layer (**14**), wherein the super lattice structure (**16**) includes a plurality of first InGaN layers and a plurality of second InGaN layers (super lattice structure **16** includes alternating layers of $In_xGa_{1-x}N$ and $In_YGa_{1-Y}N$; e.g. paragraph 49), wherein each of the plurality of first InGaN layers ($In_xGa_{1-x}N$; hereinafter "**FL**") has an In composition different (X is not equal to Y; e.g. paragraph 49) from an In composition of each of the plurality of second InGaN layers ($In_YGa_{1-Y}N$; hereinafter "**SL**"), and wherein one of the plurality of first InGaN layers (**FL**) or one of the plurality of second InGaN layers (**SL**) is directly on the first gallium nitride layer (**14**); an active layer (**18**) on the super lattice structure (**16**) including InGaN; and a second gallium nitride layer (**32**) having a second conductivity (p-type) on the active layer (**18**).

Emerson is silent as to explicitly teaching the super lattice structure including InGaN has a plurality of pits formed thereon, and wherein a non-zero number of the plurality of pits is 50 or less per area of 5μm×5μm.

Vaudo generally teaches placing a HVPE GaN **104** layer above the substrate to reduce the number of pits that propagate into subsequent layers of the device, and further teaches the super lattice structure (**16** of Emerson) including InGaN has a plurality of pits formed thereon, and wherein a non-zero number of the plurality of pits is 50 or less per area of 5μm×5μm (GaN **104** has hexagonal pit density of less than $50cm^{-2}$ which would propagate up during device layer growth; e.g. column 16, line 15-30; a density of $50cm^{-2}$ is less than a density of $25\mu m^{-2}$).

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the teachings of Vaudo in the device of Emerson and provide a HVPE layer between the substrate and the layers of the light emitting device that would allow for growth of higher quality layers that have hexagonal pit densities less than $50cm^{-2}$ (see column 16, lines 15-17 of Vaudo).

Re claim 34: Emerson teaches the LED wherein the active layer (**18**) comprises an InGaN/InGaN structure of a multi-quantum well structure (MWQ **18** made of $In_XGa_{1-X}N$ (0=<X<1); e.g. paragraph 57).

Re claim 37: Emerson teaches the LED wherein the super lattice structure (**16**) including InGaN includes an $In_xGa_{1-x}N/In_yGa_{1-y}N$ multi-layer is formed to have a super lattice structure (super lattice structure **16** includes alternating layers of $In_xGa_{1-X}N$ and $In_YGa_{1-Y}N$; e.g. paragraph 49 of Emerson).

Re claim 38: Emerson teaches the LED wherein each layer of the $In_xGa_{1-x}N/In_yGa_{1-y}N$ multi-layer has a thickness of 1-3000Å (layers of superlattice structure **16** having thickness of about 5-100 angstroms; e.g. paragraph 49).

Re claim 39: Emerson teaches the LED, wherein the super lattice structure (**16**) including InGaN has a photoluminescence characteristic of a yellow band intensity/N-doped GaN intensity ratio of 0.4 or below. Since the structure recited in the prior art is substantially identical to that of the claim, claimed properties are presumed to be present. See MPEP 2112.01(i).

Re claim 40: Emerson teaches the LED, wherein the active layer (**18**) is directly on the super lattice structure (**16**) including InGaN.

Re claim 41: Vaudo teaches the LED wherein the LED is blue LED (UV to green light emitting diodes; e.g. column 1, line 36).

Re claim 51: Emerson teaches (e.g. figure 1) a light emitting diode (LED), comprising: a substrate (**10**); a buffer layer (**11**) on the substrate (**10**); an N-type GaN layer (**14**) on the buffer layer (**11**); a super lattice structure (**16**) including InGaN directly on the N-type GaN layer (**14**), wherein the super lattice structure (**16**) including InGaN includes a plurality of first layers and a plurality of second layers (super lattice structure **16** includes alternating layers of $In_xGa_{1-X}N$ and $In_YGa_{1-Y}N$; e.g. paragraph 49), wherein each of the first layers ($In_xGa_{1-X}N$; hereinafter "**FL**") has a thickness of 1-3000Å (layers of superlattice structure **16** having thickness of about 5-100 angstroms; e.g. paragraph 49), wherein each of the second layers ($In_YGa_{1-Y}N$; hereinafter "**SL**") has a thickness of 1-3000Å (layers of superlattice structure **16** having thickness of about 5-100 angstroms; e.g. paragraph 49), and wherein one of the plurality of first layers (**FL**) or one of the plurality of second layers (**SL**) is directly on the N-type GaN layer (**14**); an active layer

(**18**) on the super lattice structure (**16**) including InGaN; and a P-type GaN layer (**32**) on the active layer (**18**).

Emerson is silent as to explicitly teaching an undoped GaN layer on the buffer layer; the N-type GaN layer directly on the undoped GaN layer; wherein the super lattice structure including InGaN has a plurality of pits thereon and wherein a non-zero number of the plurality of pits is 50 or less per area of 5μm×5μm.

Vaudo generally teaches placing a HVPE GaN **104** layer above the substrate to reduce the number of pits that propagate into subsequent layers of the device, and further teaches an undoped GaN layer (**104**) on the buffer layer (buffer layer may be grown between the layer **104** and substrate; e.g. column 11, lines 62-66); the N-type GaN layer (**106**) directly on the undoped GaN layer (**104**); wherein the super lattice structure (**16** of Emerson) including InGaN has a plurality of pits thereon and wherein a non-zero number of the plurality of pits is 50 or less per area of 5μm×5μm (GaN **104** has hexagonal pit density of less than $50cm^{-2}$ which would propagate up during device layer growth; e.g. column 16, line 15-30; a density of $50cm^{-2}$ is less than a density of $25\mu m^{-2}$).

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the teachings of Vaudo in the device of Emerson and provide a HVPE layer between the substrate and the layers of the light emitting device that would allow for growth of higher quality layers that have hexagonal pit densities less than $50cm^{-2}$ (see column 16, lines 15-17 of Vaudo).

Re claim 52: Emerson in view of Vaudo teaches the LED, further comprising: a GaN layer (**12**) between the buffer layer (**11**) and the undoped GaN layer (**104** of Vaudo). Vaudo teaches growth nucleation, buffer layer, and/or intermediate layers on the substrate before the growth of HVPE GaN layer **104**.

Re claim 53: Emerson in view of Vaudo teaches the LED, wherein the undoped GaN layer (**104** of Vaudo) is directly formed on the GaN layer (**12** of Emerson).

Re claim 54: Emerson teaches the LED wherein the active layer (**18**) comprises an InGaN/InGaN structure of a multi-quantum well structure (MWQ **18** made of $In_XGa_{1-X}N$ (0=<X<1); e.g. paragraph 57).

6. Claims 42, 44, 47-50, 55-57 are rejected under 35 U.S.C. 103(a) as being unpatentable over Emerson in view of Vaudo and Tanizawa et al. (US PGPub 2003/0205711; hereinafter "Tanizawa").

Re claim 42: Emerson teaches (e.g. figure 1) a method for manufacturing a light emitting device, the method comprising the steps of: forming a buffer layer (**11**); forming an N-type gallium nitride layer (**14**) on the buffer layer (**11**); forming a super lattice structure (**16**) including InGaN (super lattice structure **16** having alternating layers of $In_XGa_{1-X}N$ and $In_YGa_{1-Y}N$; e.g. paragraph 49) on the N-type gallium nitride layer (**14**); wherein the super lattice structure (**16**) including InGaN includes a plurality of first InGaN layers ($In_XGa_{1-X}N$; hereinafter "**FL**") and a plurality of second InGaN layers ($In_YGa_{1-Y}N$; hereinafter "**SL**"), wherein each of the plurality of first InGaN layers (**FL**) has an In composition different (X is not equal to Y; e.g. paragraph 49) from an In

composition of each of the plurality of second InGaN layers (**SL**), and wherein one of the plurality of the first InGaN layers (**FL**) or one of the plurality of second InGaN layers (**SL**) is directly on the N-type gallium nitride layer (**14**); forming an active layer (**18**) on the super lattice structure (**16**) including InGaN; and forming a P-type gallium nitride layer (**32**) on the active layer (**18**),

Emerson is silent as to explicitly teaching the super lattice structure including InGaN has a plurality of pits formed thereon, and wherein a non-zero number of the plurality of pits is 50 or less per area of 5μm x 5μm, and wherein the buffer layer is grown at a first temperature, wherein the first InGaN layer of the super lattice structure including InGaN is grown at a second temperature higher than the first temperature, wherein the second InGaN layer of the super lattice structure including InGaN is grown at a third temperature higher than the first temperature and lower than the second temperature, and wherein the active layer is grown at a fourth temperature of 600~800°C higher than the first temperature and lower than the second and third temperatures.

Vaudo teaches providing a (Ga,Al,In)N layer (hereinafter referred to as "**layer**" and labeled as **104** in figure 8) formed on a substrate with or without a buffer layer between the **layer** and substrate, wherein the **layer** allows for higher quality epitaxial growth of subsequent layers of the device (e.g. column 11, lines 63-66 and column 16, lines 26-30). Vaudo further teaches a plurality of pits (GaN **104** has hexagonal pit density of less than $50cm^{-2}$; e.g. column 16, line 15-17), and wherein a non-zero number of the plurality of pits is 50 or less per area of 5μm x 5μm (a density of $50cm^{-2}$ is

less than a density of 25μm^{-2}). The resulting structure of the combined teachings of Emerson and Vaudo would result in the super lattice structure **16** of Emerson formed on GaN **104** of Vaudo, the pits propagating up from the layer GaN **104** in substantially the same number of hexagonal pits would appear on the super lattice structure.

Tanizawa teaches the buffer layer (**2**) is grown at a first temperature (400-800˚C; e.g. paragraph 41), wherein the first InGaN layer of the super lattice structure (**6**) including InGaN is grown at a second temperature (1050˚C; e.g. paragraphs 96 and 98) higher than the first temperature (400-800˚C), wherein the second InGaN layer of the super lattice structure (**6**) including InGaN is grown at a third temperature (800˚C; e.g. paragraph 98) higher than the first temperature (400-800˚C; e.g. paragraph 41) and lower than the second temperature (800˚C; e.g. paragraph 98), and wherein the active layer (**7**) is grown at a fourth temperature of 600~800˚C higher (less than 800˚C since active layer **7** contains a higher amount of indium) than the first temperature (400-800˚C; e.g. paragraph 41) and lower than the second (800˚C) and third temperatures (1050˚C; e.g. paragraphs 96 and 98).

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the teachings of Vaudo and Tanizawa in the device of Emerson and have a base GaN layer having less than 50 pits per cm^2 allowing for a high quality epitaxial growth to be attained (see column 16, lines 29-30 of Vaudo) and use the temperature ranges for the growth of the layers as taught by Tanizawa since Emerson is silent as to the temperatures and would have the predictable result of a

manufacturing method which would result in a working device with decreased number of pits.

The combination is motivated by the teachings of Vaudo and Tanizawa who point out the advantages of using a HVPE layer and the processing temperatures for making a light emitting device.

For example, Vaudo teaches at column 16, lines 15-30 that pit densities of less than 50 cm-2 by using the HVPE layer and Tanizawa teaches at paragraph 42 that pit densities can be reduced by the method taught by the Tanizawa reference.

Re claim 44: Emerson teaches the method wherein the active layer (**18**) comprises an InGaN/InGaN structure of a multi-quantum well structure (active region **18** includes InGaN layers; e.g. paragraph 51).

Re claim 47: Emerson teaches the method wherein the super lattice structure (super lattice structure **16** having alternating layers of $In_XGa_{1-X}N$ and $In_YGa_{1-Y}N$; e.g. paragraph 49) including InGaN includes an $In_xGa_{1-x}N/In_yGa_{1-y}N$ multi-layer is formed to have a super lattice structure.

Re claim 48: Emerson teaches the method wherein each layer of the super lattice structure (**16**) including InGaN has a thickness of 1-3000Å (5-100 angstroms; e.g. paragraph 49).

Re claim 49: Emerson teaches the device wherein the super lattice structure (**16**) including InGaN has a photoluminescence characteristic of a yellow band intensity/N-doped GaN intensity ratio of 0.4 or below. Since the structure recited in the

prior art is substantially identical to that of the claim, claimed properties are presumed to be present. See MPEP 2112.01(i).

Re claim 50: Emerson teaches the active layer (**18**) being directly formed on the super lattice structure (**16**) including InGaN.

Re claim 55: Emerson in view of Vaudo teaches the method, further comprising: forming an undoped GaN layer (**104** of Vaudo) on the buffer layer (**11**) before forming the N-type gallium nitride layer (**14**).

Re claim 56: Emerson in view of Vaudo and Tanizawa teaches the method, wherein the undoped GaN layer (**104** of Vaudo) is grown at a fifth temperature (1020˚C to about 1200˚C; e.g. column 14, line 55) higher than the first temperature (400-800˚C; e.g. paragraph 41 of Tanizawa), the second temperature (800˚C; e.g. paragraph 98 of Tanizawa), the third temperature (1050˚C; e.g. paragraphs 96 and 98 of Tanizawa) and the fourth temperature (less than 800˚C).

Re claim 57: Emerson in view of Vaudo and Tanizawa teaches the method, further comprising: forming a plurality of pits (pits appear on the surface of the p-type contact layer **10** are produced from pits formed in layers below it; e.g. paragraph 33 of Tanizawa) between the active layer (**18** of Emerson) and the P-type gallium nitride layer (**32** of Emerson).

Response to Arguments

7. Applicant's arguments with respect to claims 33, 34, 37-42, 44, 47-57 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JESSE Y. MIYOSHI whose telephone number is (571)270-1629. The examiner can normally be reached on M-F 7:30AM-5:00PM EST. Alternating Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne A. Gurley can be reached on (571) 272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JYM

/Ori Nadav/
Primary Examiner, Art Unit 2811